Hall Ticket Number:

Code No. : 22606

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.E. (ECE: CBCS) II-Semester Main Examinations, July-2017

(Embedded Systems & VLSI Design)

CPLD & FPGA Architectures and Applications

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. List the limitations of FPGAs.
2. Explain difference between programmable array logic and Programmable Logic array structures.
3. Write all the features of XILINX Spartan-II FPGA.
4. Draw the architecture of 3-input Look Up Table.
5. What is macro-cell in a CPLD?
6. Explain Generic Logic Block (GLB) of lattice PLSI Architecture.
7. What are the reasons for delay in an FPGA?
8. Differentiate between global routing and detailed routing.
9. Classify and explain digital circuits' failures.
10. Highlight the importance of test pattern generation and where is it useful.

Part-B (5 × 10 = 50 Marks)
(All bits carry equal marks)

11. a) What are the various components of FPGA? Explain the same with neat diagram.
    b) Explain in detail about FPGA based system design flow.
12. a) Compare the performance parameters of ACTEL based FPGAs ACT-1, 2 and 3.
    b) Explain about Virtex-II FPGA Architecture.
13. a) Explain in detail about Altera flex logic 10000 series CPLDs.
    b) Describe the architecture of AT & T ORCA. In what way are the Cypress CPLDs differ from ORCA?
14. a) Explain Mincut based placement algorithm with example.
    b) What is routing? Explain Segmented channel routing.
15. a) Explain the different faults that occur in digital circuits.
    b) What are the various steps involved in ASIC based design? Explain them.
16. a) Discuss the Antifuse programming technology.
    b) Explain general architecture of Xilinx FPGAs.
17. Write short notes on any *two* of the following:
    a) Max 7000 Series CPLDs
    b) Simulated annealing
    c) Faults and fault coverage.